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ASIC Chip Design for Healthcare System

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Abstract—

This study introduces a RISC-V digital processing unit and sensor interface circuit solution that is well-suited for healthcare-related ASIC applications. In order to keep an eye on things or take precautions, people employ systems on chip, or SoC. Creating an application-specific integrated circuit (ASIC) to manage signal processing and computing in a healthcare system with an ultra-low-power System on Chip (SoC) architecture, tailored for use in wearable healthcare systems, with the goal of reducing processor power consumption. Two sensors, one for measuring force/pressure and the other for electrocardiogram signals, make up the design. The data collected by these sensors is used to create analog circuit designs. Implementing a processor's RTL-based design is done using Verilog HDL. We use Xilinx ISE to check for logic equivalence. By following the RTL to GDSII design pipeline, one may get physical implementations of their designs. Unity Gain Buffer, sample and holds circuit, and flash-type ADC make up the analog design. We have used Cadence CAD tools to test ASICs using AMS verification technique. In contrast to the digital ASIC, which operates at 2.85 GHz and has an area of 18088.380 µm2, the analogue ASIC has a surface area of 4,40,000 µm2 and a power dissipation of 4.4 mW. The core dissipates a total of 368 µW of power. ASIC, R-Isc, ADC, and HDL are some of the terms used to describe this.

I. INTRODUCTION

Modern healthcare has mostly relied on sensor-based systems due to their high degree of accuracy. As a tool for decision-making or health monitoring, embedded systems, including designs based on systems of circuits, are used. Wearable sensors equipped with powerful computers form the basis of such systems, which do not involve intrusive procedures [1]. The healthcare industry is only one of several that is now making use of machine learning and edge computing. Wearable technology often uses it to enhance the precision of monitoring and rapid analysis [2]. In cases when a high-quality precision healthcare system is required, it is recommended to repeatedly monitor regularly obtained data in order to enhance the prompt and correct identification of respiratory distress syndrome, particularly in its milder phases, which are often underdiagnosed [3]. In order to power wearable medical devices, we need a healthcare system that is designed with ultra-low-power System on Chip (SoC) architecture. A hardware accelerator may offload computation and process signals, reducing the processor's footprint and power usage. Additionally, in order to enhance the accelerator's performance while minimizing its space and power consumption [4]. Microprocessors, microcontrollers, PCs, mobile phones, and digital signal processors are just a few of the platforms that can handle ECG signals nowadays. The analysis of ECG signals does have certain limitations, however. Consider a discrete component system that relies on microprocessors; its performance is constrained by factors like clock speed and the intricacy of its internal architecture. Because of its sequential structure, the microcontroller's fetch-decode-execute cycle is slow while processing instructions [5]. Resulting from the lightning-fast development of edge computing for signal processing, biological sensing, and optimized ASICs [6, 7]. For systems that use wearable health devices, we want an ASIC chip design that can process ECG signals while using little power and extracting the ECG characteristics. By using AI characteristics, the new trends are used for the identification of ECG

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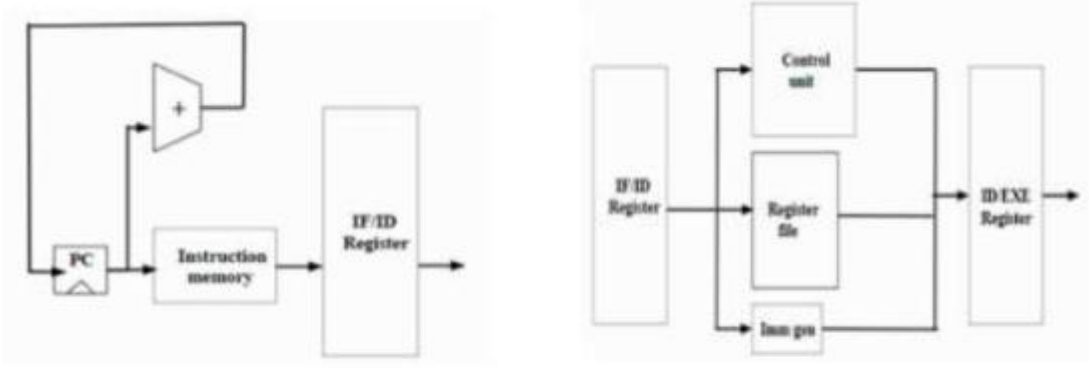
arrhythmia. For data decision-making, we need a layout including a sensor unit, analogue-to-digital converter, pre-processing step, and feature extraction step. One application-specific integrated circuit (ASIC) that processes both digital and analog electrocardiogram data [8]. We are now moving away from a clinic-centric paradigm and toward a person-centric model, or customized healthcare system, with the backing of the Internet of Things (IoT) and ancillary technologies like cloud computing and big data analytics [9]. Below is the top module of the design, which houses the designed ASIC modules needed to construct a single healthcare system on a chip (SoC). Figure 1 is the high-level implementation diagram. Create a RISC-V core using the RV32I ISA. The program that has to be executed is stored in instruction memory. Unidirectional memory is what it is. The information that is loaded or stored in memory is referred to as data memory. There is a two-way street in data memory. Specifically, these upgrades cover the digital domain, from RTL to GDSII. The analog parts include the sensor interface circuits and the analog to digital converter (ADC). Digital outputs from sensors are handled by the ADC. Starting with the digital ASIC design—which includes its physical design flow and RTL design—the next sections provide thorough information on all the implementations. The next step is the design of the analog ASIC, which includes components such as a unity gain buffer, a sample and hold circuit, a CMOS open loop comparator, a two-stage operational amplifier, etc.



(a) Instruction Fetch (b) Instruction Decode

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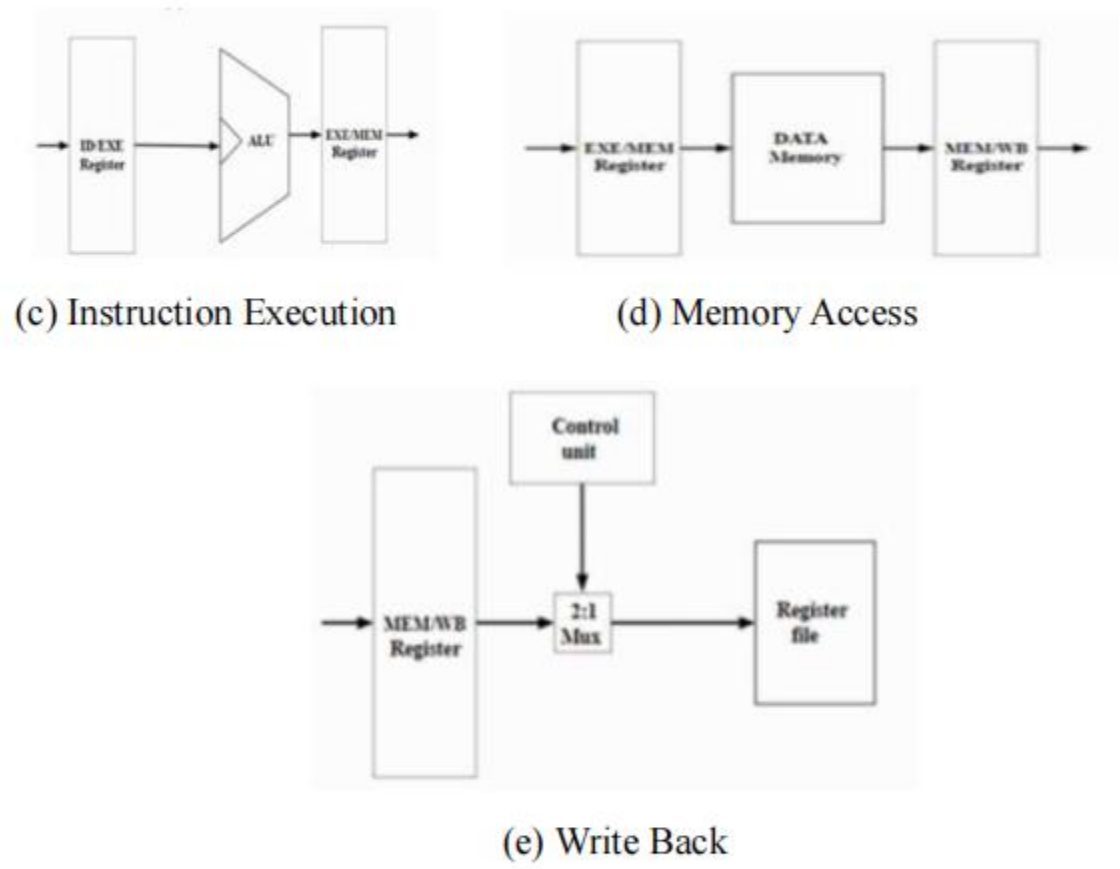

Fig. 1. Block Diagram of Proposed Healthcare ASIC System

II. DIGITAL ASIC DESIGN FOR HEALTHCARE SYSTEM

The central processing unit (CPU) of a digital ASIC is a RISC V microprocessor with five stages of pipeline processing, as well as data and instruction memory.

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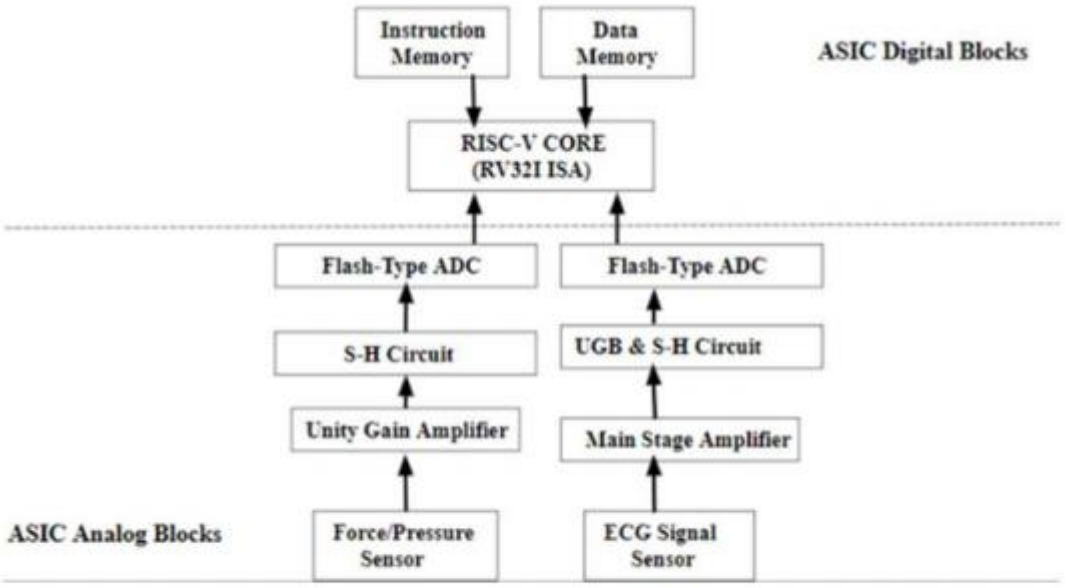

Fig. 2. Stages of the RISC-V ISA Core

A. RISC-V ISA Implementation

RISC-V is an open-source ISA that follows the tried-and-true reduced instruction set concept in computers. RISC-V is a five-stage pipeline architecture, notably Instruction Fetch Stage (IF), Instruction Decoder Stage (ID), Execution Stage (EX), Memory Access Stage (MEM), and Write Back Stage (WB). The 35–40 Instructions that make up the RV32I base version of the ISA were designed here in the microarchitecture. We used Verilog HDL to build all the functionality, and then we synthesized it for physical design flow. Using the address in memory that is stored in both the program counter and the instruction register, the following instruction is retrieved. As demonstrated in Figure 2, the IF stage instruction is retrieved and the Program Counter (PC) is increased by a factor of four. At this point, the decoder reads the instruction register and deciphers the encoded instruction. In the ID stage, if the instruction in the IR is not a jump (j, jal, or jr), Sign extended immediate or offset values calculation and applies to the execution EX stage as shown in Fig.2. ALU and updated the necessary flags or effective addresses are also computed inside the same blocks by distinguishing ALUsrc and ALUop as illustrated in Fig.2. The load and store instructions at this step come into the picture where the blocks which are utilized out of the whole data stream are presented Fig.2. For all the instructions where the ultimate destination register where this stage put the results within the destination register which is identified at the instruction decoder stage. Normally R-type/Load-type/J-type instructions will be impacting this stage and its microarchitecture are depicted in Fig.2. Here provided design micro architecture in a manner that it detects risks using a hazard detection unit if any happened either Read After Write (RAW) or Write After Write (WAW). Normally hazards interrupts execution and produce inaccurate computation results. A synthesis tool will transform RTL into a set of interconnected logic gates that define the logic. The most common format is Verilog. Standard Cell Library will include a layout and timing model information for the Standard cells. The rules concerning the procedure that has been chosen should also be given to the PNR tool. This contains metal widths, spacing, definitions, etc. SDC files establish the time restrictions of your design. Definitions

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of the clock, false pathways, limitations on input and output delays, etc., will be at your disposal. As far as the layout is concerned, this is the first major phase. Chip quality is determined by the floor layout. Here you may set the general chip/block size, assign power routing resources, locate the hard macros, and set aside room for regular cells. The physical design and verification phases are essential to the development of any application-specific integrated circuit (ASIC) or system-on-chip (SoC) because they give form to the first chip blueprint. It will be sent to the fabrication house after all signoffs are complete.

III. ANALOG ASIC DESIGN FOR SENSOR INTERFACING

The physical design flow of an ASIC begins with a logical description of the hardware and continues through phases such as synthesis, floor-planning, placement, routing, and verification before the design is ready for semiconductor production. A wide variety of sensor interface circuits are found in analog ASICs, including Op-Amps, Unity Gain Buffers (UGBs), Sample and Hold circuits, Flash type ADCs, and many more. You will find an in-depth study and description of the Analog ASIC system and its constituent parts in the sections that follow. Part A: Operational Amplifier for CMOS. The design of many analog and mixed-signal circuits relies on operational amplifiers (Op-Amps). The characteristics of the ADCs' circuit design, as well as the specifications of the Sample and Holds, were used to create the Op-Amp, as given in Table.Figure 3 shows the basic layout of a two-stage operational amplifier, which includes a differential amplifier and a common source amplifier.

TABLE I. TWO STAGE CMOS OP-AMP SPECIFICATIONS

Sr. No.	Design Parameter	Values
1	Supply Voltage	1.8 V
2	Biasing Current	16 µA
3	Open-loop Gain	70-75 dB
4	Gain-Bandwidth Product	10 MHz
5	Slew Rate	10 V/µs
6	ICMR	0.8 to 1.6
7	CMRR	> 60 dB
8	PSRR	> 60 dB
9	Output Swing	It depends upon the load
10	Power Dissipation	< 1 mW

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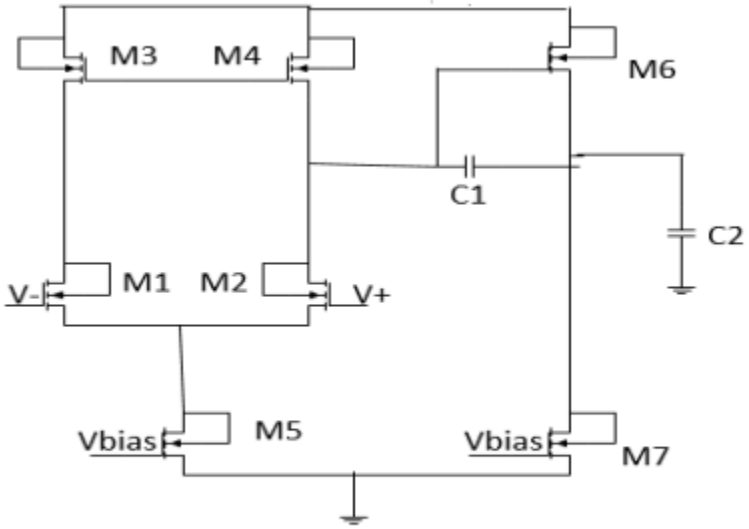

Fig. 3. Two Stage CMOS Op-Amp

B. Design Procedure of Op-Amp

There are a number of design considerations that must be considered while creating a two-stage CMOS Op-amp. A CMOS op-amp's transistors may be appropriately sized with the aid of these design procedures. Assuming z > 10 GB, use the equation to get the value of Cc for the required phase margin (PM) of 60 degrees.

$$C_c > 0.22C_L \qquad (1)$$

Determine the tail current I5 using the equation as shown below,

$$I_5 = SR.\,C_c \qquad (2)$$

Design for M1 from maximum input voltage specifications, given by the equation

$$\left(\frac{W}{L}\right)_3 = \frac{I_5}{(K_3)\{V_{dd} - V_{in}(max) - V_{t03}(max) + V_{t1}(min)\}^2} \qquad (3)$$

Verify that the pole and zero due to Cgs3 and Cgs4 will not dominate by assuming P3 > 10 GB,

$$\frac{gm_3}{2\times C_{gs_3}} > 10.\,GB \qquad (4)$$

Design for M1 and M2 so as to achieve desired GB

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$$gm_1 = GB \times C_c \quad (5)$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{(gm_2)^2}{K_2.I_5} \quad (6)$$

Design for M5 by first calculating Vds5(sat) as given by below equation,

$$V_{ds5}(sat) = V_{in}(min) - V_{ss} - \frac{I_5}{B_1} - V_{t1}(max) \geq 100mV \quad (7)$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{(K_5[V_{ds5}(sat)^2]^2)} \quad (8)$$

Design for S6 by letting p2 ≥ 2.2.GB

$$gm_6 = 2.gm_2\left(C_L/C_c\right) \quad (9)$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \left(gm_6/gm_4\right) \quad (10)$$

Now solve for I6 as given by the equation

$$I_6 = \left(gm_6^2/2K_6S_6\right) \quad (11)$$

Design for S7 as given by the equation

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 \left(I_6/I_5\right) \quad (12)$$

Check for gain and power dissipation as given by equation,

$$A_v = \frac{2gm_2gm_6}{\{I_5(\lambda_2+\lambda_3)I_6(\lambda_6+\lambda_7)\}} \quad (13)$$

$$P_{diss} = (I_5 + I_6).(V_{dd} + V_{ss}) \quad (14)$$

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Based on the above equations and specifications given in Table 1, W/L ratios for the MOSFETS of the Op-Amp is given in Table 2.

TABLE II. OP-AMP EACH MOSFET'S W/L RATIO

M1,M2	2
M3,M4	10
M5,M8	44
M6	48
M7	100

C. Design Procedure of CMOS Comparator

A comparator is a circuit that takes in two analogue signals, compares them to a reference signal, and then produces a binary signal depending on the outcomes of the comparison. The conversion of analog signals to digital converters is the primary use of the comparator. Before doing UGB in an analog-to-digital conversion, it is required to sample the input. The digital version of the analogue signal is obtained by applying the sampled signal to a set of comparators. The comparator, at its most basic, is an analog-to-digital converter with one bit of input. Below Fig.4 is a CMOS open-loop comparator.

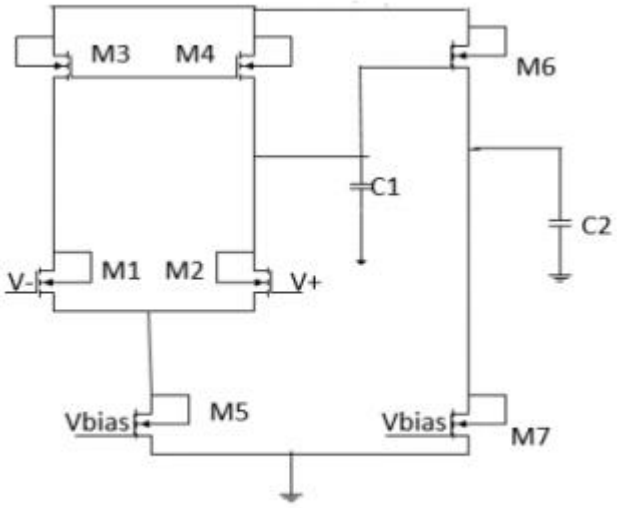

Fig. 4. Two Stage CMOS Comparator

CMOS comparator is also designed based upon standard equation which are given below,

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$$|PI| = |PII| = \frac{1}{tp\sqrt{mk}} \quad (15)$$

$$I_7 = I_6 = \frac{|PII|CII}{\Delta n + \Delta p} \quad (16)$$

$$\left(\frac{W}{L}\right)_6 = \frac{2.I_6}{K_6(V_{ds6}(sat))^2} \quad (17)$$

$$\left(\frac{W}{L}\right)_7 = \frac{2.I_7}{K_7(V_{ds7}(sat))^2} \quad (18)$$

Suppose, CI as 0.1-0.5 pF; I5 = I7.2CI/CII

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{K_3(V_{gs3}-V_{tp})^2} \quad (19)$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(gm_2)^2}{K_2.I_5} \quad (20)$$

$$V_{ds5}(sat) = V_{icm}(-) - V_{gs1} - V_{ss} \quad (21)$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{(K)_5[V_{ds5}(sat)^2]^2} \quad (22)$$

Table 3 displays the W/L ratios for the MOSFETS in the Comparator Circuit, which are derived from the parameters and formulae provided in Table 1.

TABLE III. MOSFET'S W/L RATIO FOR COMPARATOR CIRCUIT

M1,M2	8
M3,M4	10
M5,M8	15
M6	272
M7	136

D. Others Analog Component Design

Prior to creating the complete flash-type ADC, additional components such the Unity Gain Buffer (UGB) and sample and hold are necessary. Here you will find comprehensive data accompanied with design equations. The Unity Gain Buffer, seen in Fig.5, is an example of an Op-Amp design.

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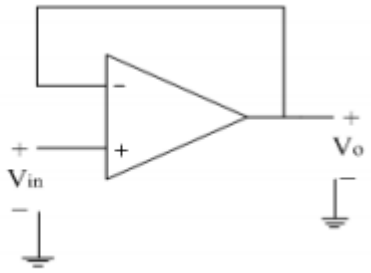

Fig. 5. Unity Gain Buffer (UGB)

Since the usual equation of the non-inverting Op-Amp is provided below, Fig. 5 may be used as a unity gain in this case.

$$V_{out} = \left(1 + \frac{R_f}{R_1}\right) V_{in} \qquad (23)$$

Vout=Vin if and only if Rf and R1 are both zero. A similar sample-and-hold circuit using a high-gain operational amplifier (op-amp) and a single NMOS switch for operation and hold capacitor control is shown in Figure 6. The setup works like this: the capacitor begins charging while the NMOS switch is on hold, and it transfers charging to the final unity gain amplifier when the switch is off. Compared to the subsequent circuits, this one is quicker since there is no feedback. However, closed-loop designs provide better accuracy metrics because to their feedback. As little time as feasible must be spent on acquisition. Three things must be considered: The maximum output current is dependent upon the slew rate of the opto amplifier, and the RC time constant is defined as the product of the ON resistance of the MOSFETs and the holding capacitor CH. E. Designing and Verifying the Functionality of the ADC Because of its superior performance in comparison to other architectures in this regard, the flash-type ADC should be the aim here. Figure 7 shows the basic layout of an ADC, which includes a comparator array and a priority encoder. As demonstrated in Figure 9, the AMS verification cadence tools offer the ability to validate functionality through the use of its standard methodology. This methodology entails designing a 64 to 6 priority encoder in Verilog HDL, creating a symbol for it, and then designing the entire ADC structure.

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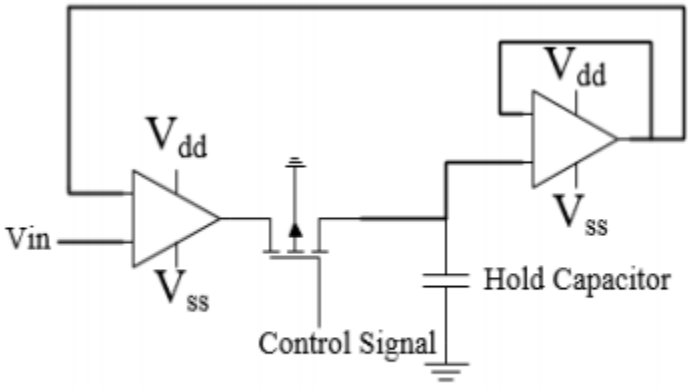

Fig. 6. Sample And Hold Circuit Design

It has also been tested for different input sample values to ensure it works as expected and has logical equivalence. We have created a 6-bit exploration approach for the development of ASICs and AMS designs.

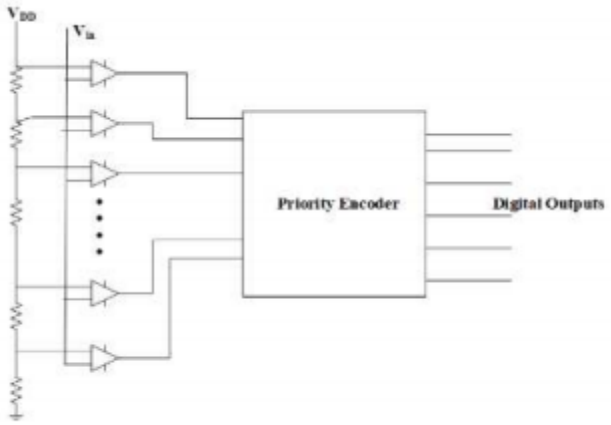

Fig. 7. Flash-Type ADC Diagram

Here, the provided 6-bit ADC is based upon the accuracy that is needed for appropriate sensor interface; further component assembly is then required according to the above block diagram. The results section displays the cadence AMS verification mythology, which is used to verify the operation of the ADC.

IV. RESULTS AND ANALYSIS

Using Xilinx ISE, as shown in Fig. 8(a,b) below, we first made sure the RISC-V ISA worked as intended and that its logical equivalence was correct. We then built two memory modules to test it, and we put a few different combinations of instructions and data into each one. The results of the tests were within our expectations. Following the completion of the functional simulation, we used Cadence tools (Genus/Innovus) to execute its full PD flow. This included doing pre- and post-synthesis analysis, leading to the validated final core layout, as shown in Figure 9. Table displays the findings for the performance parameters.4.

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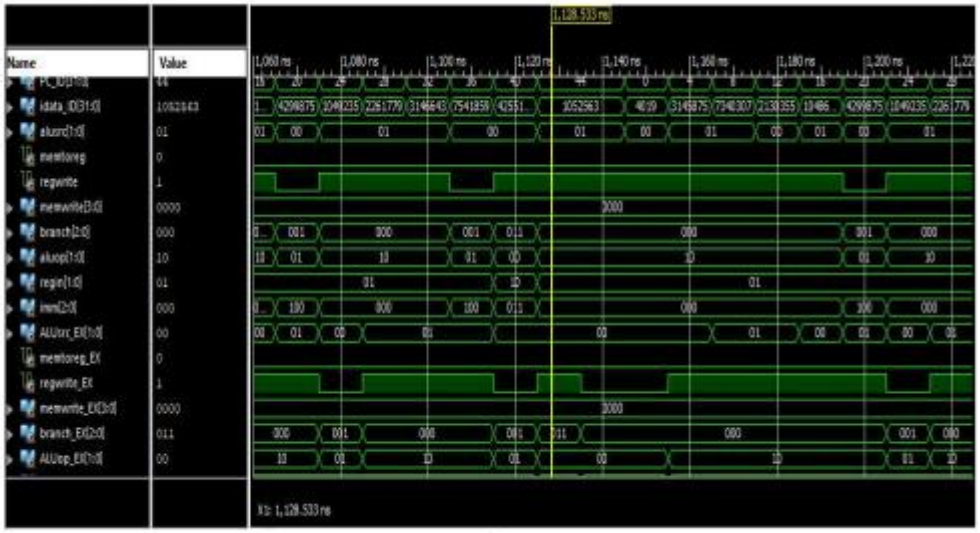

(a)

(b)

Fig. 8. Functionality Verification of RISC-V core (a) RTL Simulation (b) RTL Simulation (cont'd)

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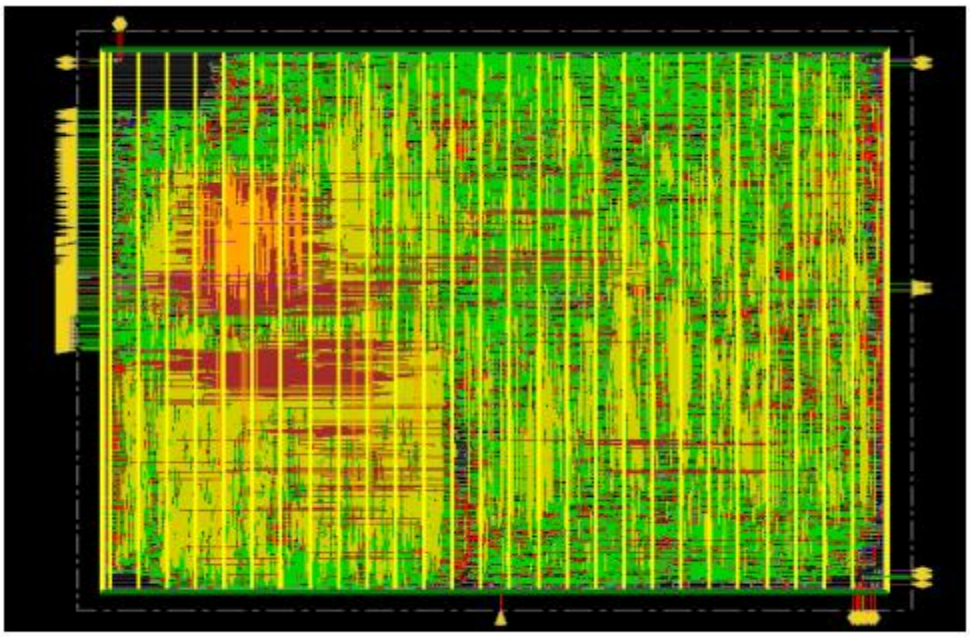

Fig. 9. Final Layout of RISC-V Core

Starting the analog ASIC from the Op-Amp allows us to see its frequency response and transient simulation in Figures 10 and 11. Fig.12 shows the AC analysis of the Op-Amp with a capacitive load; the specified values for DC gain (70–75 dB) and phase margin (62.5 degrees) are met. Also displayed in Fig.12 is the transient simulation of a two-stage CMOS comparator that is open-loop developed. The current driving capacity of a Flash-Type ADC is provided by a Unity Gain Buffer and the Sample And Hold (S-H) circuit. Figure 13 displays the outcomes of their simulation. The sample-and-hold circuit, comparator, unity gain buffer, two-stage CMOS opto-amp, and final architecture are all depicted in Fig.14.

TABLE IV. SPECIFICATION OBTAINED

Parameter	Value
Area (μm^2)	18088.380
Frequency (GHz)	2.85
Power Dissipation (μW)	368

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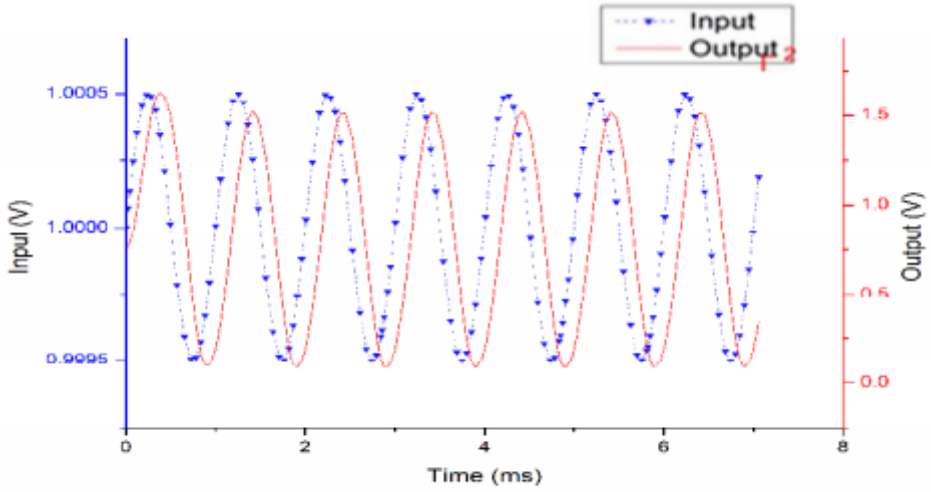

Fig. 10. Transient Simulation of CMOS Op-Amp

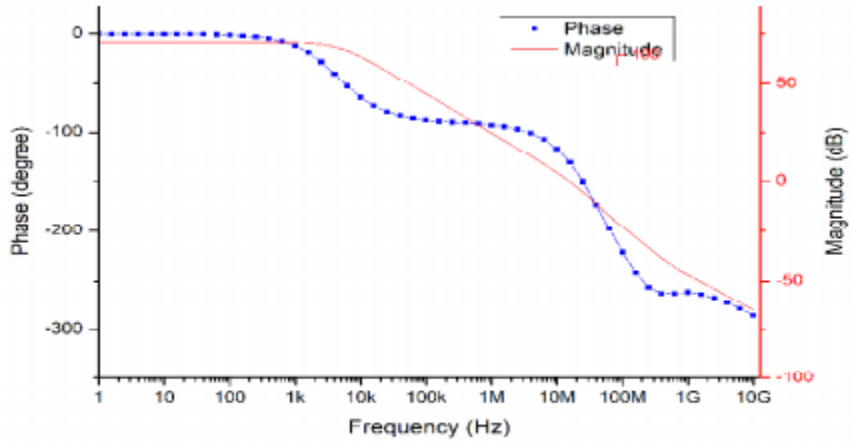

Fig. 11. AC Analysis of CMOS Op-Amp

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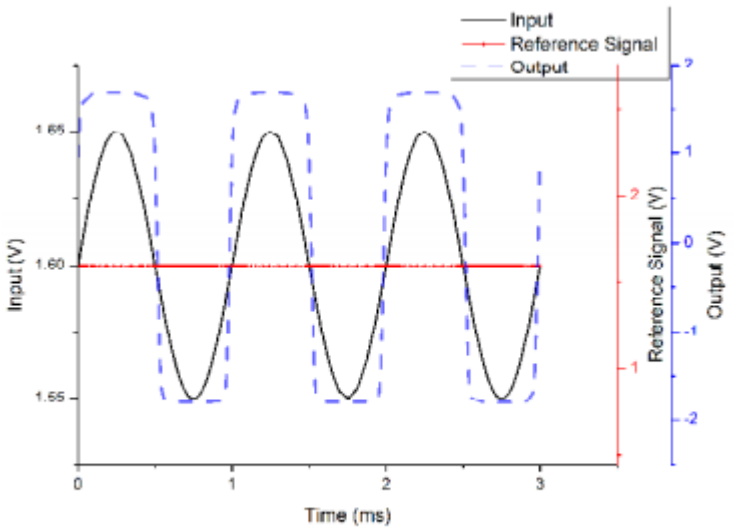

Fig. 12. Transient Analysis of CMOS Comparator

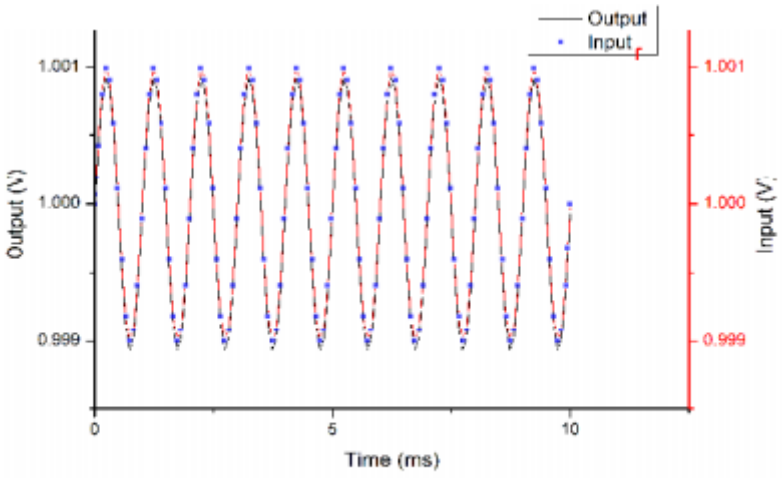

Fig. 13. Transient Simulation of Unity Gain Buffer

The RISC-V core and the Analog ASIC are compared in Table.5, while Table.6 illustrates the results. The table shows that an Analog ASIC and RISC-V core outperform previous efforts in terms of power and latency.

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TABLE V. COMPARISON OF PROPOSED RISC-V CORE

Sr. No.	This Work	[10]	[11]	[12]	[13]
Technology	45nm	65nm & 130 nm	130 nm	FPGA	FPGA
Instruction Set	RV32I	RV32I	RV32IMC	RV32I	RV32I
Pipeline Stages	5	5	5	5	5
Area (μm^2)	18088.38	-	200000	-	-
Power (μW)	368	600	500	2650	4500
Critical Path Delay (ps)	350	1250	2000	31250	29800

TABLE VI. COMPARISON OF PROPOSED ANALOG ASIC

Sr. No.	This Work	[14]	[15]	[16]
Technology (nm)	180	180	180	180
Gain Bandwidth (MHz)	10	30	34	-
Gain (dB)	72	67.5	65	-
Power (μW)	368	600	500	2650
Propagation Delay (ns)	250	-	-	300
Phase Margin (Degree)	62.5	60	65	-
Area (μm^2)	4,40,000	-	-	-

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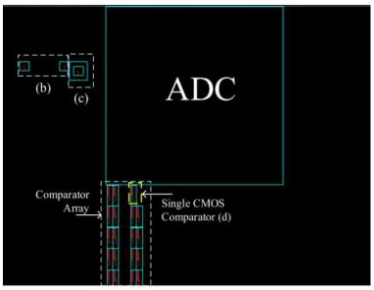
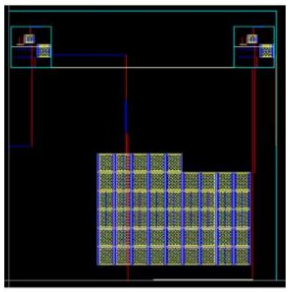
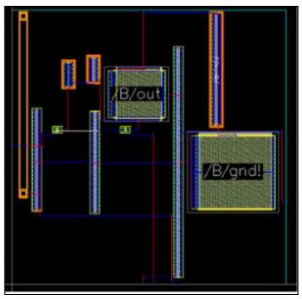


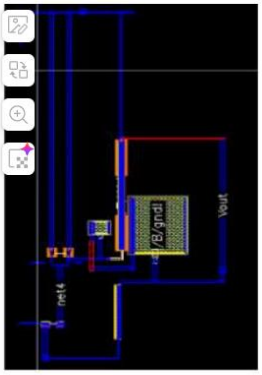
(a) 6-bit ADC cross section



(b) Sample and Hold circuit layout



(c) Op-Amp



(d) Comparator

V. CONCLUSION AND FUTURE SCOPE

Electronics will play a significant role in the healthcare system of the future. Advancements in integrated circuit design are the only thing that can pave the way for healthcare to move away from hospitals and toward home care and consumer wearables. Advanced system on a chip (ASIC) technology is essential as chips become smarter, smaller, quicker, and have longer battery lives on a single charge. Here we provide two distinct analog and digital system blocks, each with its own custom-designed ASIC. The whole system's digital ASIC operates at 2.85 GHz, and its digital core has an area of 18088.380 µm2. With a total size of 4,40,000 µm2 and a power dissipation of 4.4 mW, the analog ASIC has a total power dissipation of 368 µW in the core. Due to RISC V ISA, it will be able to perform the machine learning algorithms for the sensor's processing. With the help of the ASICs we're proposing, we can build the system on a chip (SoC) for a fully working healthcare system, replete with Internet of Things (IoT) components that allow for wireless communication.

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